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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,296	04/30/2001	Aaron W. Buchwald	1875.0560002	1034

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,296	BUCHWALD ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-9/01 6-7/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statements (IDS) are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: ***fig. 10, ref. 1000 and fig. 9, refs. 910a-d***. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 1 recites the limitation "the received data signal" in line 6. There is insufficient antecedent basis for this limitation in the claim.

5. Claims 24 and 25 are based upon the method claim 23 and should not refer to "the system of claim 23".

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 9 and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 9 and 22, the specification does not enable one skilled in the art to "rotate the interpolated phase of the sampling signal **at a rate corresponding to the frequency offset**". The specification is related to the phase alignment of a data signal with a sampling signal. The specification does not relate to or enable one skilled in the art to modify any frequencies. Further, the rotation of the interpolated phase output signal does not occur according to the "rate of the frequency offset" as claimed. The rate at which the interpolated output is *adjusted or updated* is most clearly understood to be at the rate of the sampling frequency according to the drawings. However, the specification does not enable one to adjust or update the interpolated output according to the *rate of the* ***frequency offset***.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Evans et al (US 6002279 – IDS paper no. 6 ref. AE1; hereafter "Evans").

Regarding claim 1, Evans discloses by figure 3 a system for recovering timing information from a serial data signal (abstract), comprising: a phase interpolator (304; col. 4, lines 22-25) adapted to produce a timing signal having an interpolated phase responsive to a plurality of phase control signals (inputs to DACS 312; col. 4, lines 40-60); a phase controller (306; col. 4, lines 60-65; col. 5, lines 5-16) adapted to derive a rotator control signal (UP/DOWN) based on a phase offset between the received data signal (DATA) and the timing signal (RECOVERED CLOCK); and a phase control signal rotator (308 and 310) adapted to rotate the plurality of phase control signals and correspondingly the interpolated phase of the timing signal in response to the rotator control signal (col. 5, line 59 – col. 6, line 13).

Regarding claim 2, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses that the phase controller is adapted to cause the phase control signal rotator to rotate the plurality of phase control signals (col. 5, line 59 – col. 6, line 13) and correspondingly the interpolated phase of the timing signal in a direction to reduce the phase offset (col. 5, lines 5-16) between the received data signal and the timing signal (fig. 10, col. 6, lines 29-35).

Regarding claim 3, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses (col. 5, lines 5-16) that the rotator control signal is one of a phase-advance (D1=D2<>D3), a phase-retard (D1<>D2=D3), and a phase-hold signal (D1=D2=D3), the phase control signal rotator being adapted to: rotate the plurality of phase controls signals in a first direction to advance the interpolated phase of the timing signal in response to the phase-advance signal (col. 5, line 63 – col. 6, line 2); rotate the plurality of phase controls signals in a second direction to retard the interpolated phase in response to the phase-retard signal (col. 6, lines 2-3); and prevent the plurality of phase control signals and correspondingly the interpolated phase from rotating in response to the phase-hold signal (col. 6, lines 4-6).

Regarding claim 4, Evans discloses the limitations of claim 3 as applied above. Further, Evans discloses that the phase control signal rotator includes a ring of storage elements (fig. 9, ref. 902) each adapted to store one of the plurality of phase control signals, the rotator being adapted to: concurrently shift in the first direction each of the phase control signals from a present storage element to an adjacent storage element in response to the phase-advance signal; and concurrently shift in the second direction each of the phase control signals from the present storage element to an adjacent storage element in response to the phase-retard signal (col. 5, line 59 – col. 6, line 13). The bi-directional shift register (902 accompanied by 906 gray counter and 904 control logic) of Evans is a ring of storage elements because the up and down signals "wrap" around the shift register if a plurality of the same "UP" or "DOWN" pulses cause the shift register to be filled. Evans discloses that upon the filling of the shift register by 1's in the

case that a plurality of "UP" pulses are received, the register will "reverse directions" and fill with 0's. Further, the gray counter (fig. 9, ref. 906) keeps track of the overflow of the shift register (col. 6, lines 7-10). Thereby, a type of ring of storage is made by the combination of the gray counter and the shift register according to the truth table of figure 10.

Regarding claim 5, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses that each of the plurality of phase control signals is a digital signal (fig. 10).

Regarding claim 6, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses that the phase control signal rotator is a circular shift register (fig. 9, ref. 902) including one of: a plurality of linearly arranged storage cells (fig. 9, cells D1[7-0], D2[0-7], D3[7-0], and D4[0-7]) each adapted to store a respective one of the plurality of phase control signals; and a plurality of storage cells arranged in a matrix of rows and columns and linked together to form a ring structure, each of the storage cells being adapted to store a respective one of the plurality of phase control signals. The four linearly arranged groups of storage cells (D1[7-0], D2[0-7], D3[7-0], and D4[0-7]) also arrange to make a matrix of rows and columns as shown in figure 9, and they each store a respective one of the plurality of phase control signals the outputs of which are shown in figure 10 as inputs to the DACs.

Regarding claim 7, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses that the control signal rotator is adapted to cause the phase

interpolator to rotate the interpolated phase of the timing signal to one of a plurality of discrete phase values spanning a phase range of 360.degree (col. 4, lines 40-60).

Regarding claim 8, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses that the phase controller includes: a sampler adapted to sample the serial data signal according to the timing signal (fig. 3, ref. 306), thereby producing serial data signal samples (fig. 3, "RECOVERED DATA"); a phase detector adapted to derive a phase error signal indicative of the phase offset between the timing signal and the serial data signal based on the serial data signal samples (fig. 3, ref. 306; col. 4, lines 60-65); and a phase error processor adapted to derive the rotator control signal based on the phase error signal (col. 5, lines 5-16).

Regarding claim 9, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses that the phase controller and the phase control signal rotator are adapted to cause the phase interpolator to rotate the timing signal phase corresponding to a frequency offset between a frequency of the timing signal and a frequency of the serial data signal so as to frequency synchronize the timing signal to the serial data signal (col. 4, line 66 – col. 5, line 16). The purpose of the system of Evans is to frequency synchronize the timing signal by phase interpolation to the serial data signal (abstract).

Regarding claim 10, Evans discloses the limitations of claim 1 as applied above. Further, Evans discloses that the phase interpolator includes: a plurality of reference stages (fig. 5, refs. 502, 504, 506, and 508) adapted to control individual magnitudes of a plurality of component signals having different phases responsive to the plurality of

phase control signals (col. 4, lines 30-40); and a combining node (fig. 5, ref. 510) adapted to combine the plurality of component signals into the interpolated timing signal.

Regarding claim 11, Evans discloses the limitations of claim 10 as applied above. Further, Evans discloses that the plurality of component signals includes four component signals having successive phases separated at intervals of 90.degree (col. 4, lines 19-25).

Regarding claim 12, Evans discloses the limitations of claim 10 as applied above. Further, Evans discloses that the magnitude of at least one of the component signals is varied from a zero magnitude value to a maximum magnitude value in accordance with the plurality of phase control signals (col. 4, lines 40-60; fig. 10). Figure 10 of Evans shows how each of the 4 digital input words to the digital to analog converters (D_x[7:0]) vary from a zero magnitude value to a maximum magnitude value.

Regarding claim 13, Evans discloses the limitations of claim 10 as applied above. Further, Evans discloses by figure 9 that the plurality of phase control signals are subdivided into a plurality of signal sets (D1[7-0], D2[0-7], D3[7-0], and D4[0-7]), each of the signal sets being used to control the magnitude of a corresponding one of the plurality of component signals (digital to analog converter input sets D1-D4[7:0] each control one of the component signals), the phase rotator including a ring of storage elements subdivided into a plurality of ring segments (D1, D2, D3, and D4 sets), each of the ring segments being adapted to store a corresponding one of the plurality of signal sets, whereby each of the ring segments controls the magnitude of a corresponding one

of the plurality of component signals (fig. 5). The matrix comprised of the signal sets of figure 9 are used as signal set groups to the inputs of the digital to analog converters of figure 5 which each control a corresponding one of the plurality of component signals to the phase interpolator to create a phase interpolated output according to figure 5 and figure 10. Figure 5 shows the composition of the phase interpolator with the plurality of component signals, and figure 10 illustrates how the plurality of signal sets used as inputs to the phase interpolator determine the interpolated signal output.

Regarding claim 14, Evans discloses the limitations of claim 10 as applied above. Further, Evans discloses by figure 9 that the plurality of phase control signals is subdivided into a plurality of signal sets (D1[7-0], D2[0-7], D3[7-0], and D4[0-7]), each of the signal sets being applied to a corresponding one of the plurality of reference stages (digital to analog converter input sets D1-D4[7:0] each control one of the component signals), each of the plurality of reference stages (fig. 5, refs. 502, 504, 506, and 508) being adapted to control a corresponding one of the plurality of component signals in response to the corresponding signal sets (col. 4, lines 30-40).

Regarding claim 15, Evans discloses by figure 3 a system for recovering timing information from a serial data signal (abstract), comprising: a phase interpolator (304; col. 4, lines 22-25) adapted to produce a timing signal having an interpolated phase in accordance with a plurality of phase control signals (inputs to DACS 312; col. 4, lines 40-60); a sampler (fig. 3, ref. 306) adapted to sample the serial data signal according to the timing signal, thereby producing serial data signal samples (fig. 3, "RECOVERED DATA"); a phase detector (306; col. 4, lines 60-65; col. 5, lines 5-16) adapted to detect

a phase offset between the timing signal and the serial data signal based on the serial data signal samples; an interpolator controller (308) adapted to derive a rotator control signal based on the phase offset; and a phase control signal rotator (310) adapted to rotate the plurality of phase control signals and correspondingly the interpolated phase of the timing signal so as to reduce the phase offset between the timing signal and the serial data signal (col. 5, lines 5-16). Reference 306 of figure 3 "UP/DOWN DETECT" of Evans is both a sampler (fig. 7C) because it recovers the digital data as well as a phase detector (fig. 7B) because it detects a lead or lag relationship between the input signal and the recovered clock signal. The interpolator controller divides the UP/DOWN signals from the phase detector to derive a rotator control signal based on the phase offset which is input to the phase control signal rotator (fig. 9) which is adapted to rotate the plurality of phase control signals and correspondingly the interpolated phase of the timing signal so as to reduce the phase offset between the timing signal and the serial data signal (col. 5, lines 5-16; fig. 10, col. 6, lines 29-35).

Regarding claim 16, Evans discloses a method of recovering timing information from a serial data signal (abstract), comprising: (a) deriving a timing signal having an interpolated phase in response to a plurality of phase control signals (304; col. 4, lines 22-25); (b) deriving a rotator control signal (col. 5, line 59 – col. 6, line 13) based on a phase offset between the received data signal and the timing signal; and (c) rotating the plurality of phase control signals and correspondingly the interpolated phase of the timing signal in response to the rotator control signal (fig. 10, col. 6, lines 29-35).

Regarding claim 17, Evans discloses the limitations of claim 16 as applied above. Further Evans discloses rotating the plurality of phase control signals and correspondingly the interpolated phase of the timing signal in a direction to reduce the phase offset between the received data signal and the timing signal (col. 4, line 66 – col. 5, line 16). The purpose of the system of Evans is to frequency synchronize the timing signal by phase interpolation to the serial data signal (abstract).

Regarding claim 18, Evans discloses the limitations of claim 16 as applied above. Further Evans discloses (col. 5, lines 5-16) that the rotator control signal is one of a phase-advance (D1=D2<>D3), a phase-retard (D1<>D2=D3), and a phase-hold signal (D1=D2=D3), and step (c) comprises: rotating the plurality of phase controls signals in a first direction to advance the interpolated phase of the timing signal in response to the phase-advance signal (col. 5, line 63 – col. 6, line 2); rotate the plurality of phase controls signals in a second direction to retard the interpolated phase in response to the phase-retard signal (col. 6, lines 2-3); and prevent the plurality of phase control signals and correspondingly the interpolated phase from rotating in response to the phase-hold signal (col. 6, lines 4-6).

Regarding claim 19, Evans discloses the limitations of claim 16 as applied above. Further, Evans discloses that each of the plurality of phase control signals is a digital signal (fig. 10).

Regarding claim 20, Evans discloses the limitations of claim 16 as applied above. Further, Evans discloses that step (c) comprises rotating the interpolated phase of the

timing signal to one of a plurality of discrete phase values spanning a phase range of 360.degree (col. 4, lines 40-60).

Regarding claim 21, Evans discloses the limitations of claim 16 as applied above. Further, Evans discloses that step (b) comprises: sampling the serial data signal according to the timing signal (fig. 3, ref. 306), thereby producing serial data signal samples (fig. 3, "RECOVERED DATA"); deriving a phase error signal indicative of the phase offset between the timing signal and the serial data signal based on the serial data signal samples (fig. 3, ref. 306; col. 4, lines 60-65); and deriving the rotator control signal based on the phase error signal (col. 5, lines 5-16).

Regarding claim 22, Evans discloses the limitations of claim 16 as applied above. Further, Evans discloses rotating the interpolated phase of the timing signal at a rate corresponding to a frequency offset between a frequency of the timing signal and a frequency of the serial data signal so to frequency synchronize the serial data signal to the timing signal (col. 4, line 66 – col. 5, line 16). The purpose of the system of Evans is to frequency synchronize the timing signal by phase interpolation to the serial data signal (abstract).

Regarding claim 23, Evans the limitations of claim 16 as applied above. Further, Evans discloses by figure 5 that step (a) comprises: controlling individual magnitudes (502, 504, 506, 508) of a plurality of component signals having different phases responsive to the plurality of phase control signals; and combining (510) the plurality of component signals into the interpolated timing signal (col. 4, lines 40-60; fig. 10). Figure

10 of Evans shows how each of the 4 digital input words to the digital to analog converters (D_x[7:0]) vary from a zero magnitude value to a maximum magnitude value.

Regarding claim 24, Evans the limitations of claim 23 as applied above. Further, Evans discloses that said controlling step comprises controlling individual magnitudes of four component signals having successive phases separated at intervals of 90.degree (col. 4, lines 19-25).

Regarding claim 25, Evans the limitations of claim 23 as applied above. Further, Evans discloses that said controlling step comprises varying the magnitude of at least one of the component signals from a zero magnitude value to a maximum magnitude value in accordance with the plurality of phase control signals (col. 4, lines 40-60; fig. 10). Figure 10 of Evans shows how each of the 4 digital input words to the digital to analog converters (D_x[7:0]) vary from a zero magnitude value to a maximum magnitude value.

Regarding claim 26, Evans discloses by figure 3 a method for recovering timing information from a serial data signal (abstract), comprising: producing a timing signal (304; col. 4, lines 22-25) having an interpolated phase in accordance with a plurality of phase control signals (inputs to DACS 312; col. 4, lines 40-60); sampling the serial data signal (fig. 3, ref. 306) according to the timing signal, thereby producing serial data signal samples (fig. 3, "RECOVERED DATA"); detecting a phase offset between the timing signal and the serial data signal based on the serial data signal samples (306; col. 4, lines 60-65; col. 5, lines 5-16); deriving a rotator control signal based on the phase offset (308); and rotating the plurality of phase control signals (310) and

correspondingly the interpolated phase of the timing signal in response to the rotator control signal so as to reduce the phase offset between the timing signal and the serial data signal (col. 5, lines 5-16). Reference 306 of figure 3 "UP/DOWN DETECT" of Evans is both a sampler (fig. 7C) because it recovers the digital data as well as a phase detector (fig. 7B) because it detects a lead or lag relationship between the input signal and the recovered clock signal. The interpolator controller divides the UP/DOWN signals from the phase detector to derive a rotator control signal based on the phase offset which is input to the phase control signal rotator (fig. 9) which is adapted to rotate the plurality of phase control signals and correspondingly the interpolated phase of the timing signal so as to reduce the phase offset between the timing signal and the serial data signal (col. 5, lines 5-16; fig. 10, col. 6, lines 29-35).

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending

Application No. 09/844432. Although the conflicting claims are not identical, they are not patentably distinct from each other because the broader claim 1 of the instant application would be obvious in view of the narrower claim 1 of Application No. 09/844432 (hereafter '432). Claim 1 of the instant application recites the limitation "a phase interpolator adapted to produce a timing signal", and claim 1 of '432 recites "a phase interpolator adapted to derive a sampling signal". The generation of a timing signal is equivalent to the generation of a sampling signal. Claim 1 of the instant application recites the limitation "a phase controller adapted to derive a rotator control signal", and claim 1 of '432 recites "a controller ... adapted to generate a rotator control signal". It is obvious that the controller of '432 is a "phase" controller. The additional limitations regarding the controller in claim 1 of '432 are not present in the phase controller of the instant application, and therefore, claim 1 of the instant application merely broadens the scope of claim 1 of '432. Further, claim 1 of the instant application includes "a phase control signal rotator adapted to rotate the plurality of phase control signals in response to the rotator control signal" while claim 1 of '432 includes "a control signal rotator adapted to manipulate the control signals in response to the rotator control signal". It is obvious the limitations of claim 1 of '432 read on the limitations of claim 1 of the instant application. Further, it has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same functions as before. See *In re Karlson*, 136 USPQ 184 (CCPA 1963). Also note *Ex Parte Rainu*, 168 USPQ 375 (BdPatApp&Int 1970); omission of a reference element whose function is not needed would be obvious to one skilled in the art. In this case,

the omission of some elements of the [phase] controller of claim 1 of '432 is held to be obvious because the remaining elements perform the same function as claim 1 of the instant application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art not relied upon above is cited to further show the state of the art with respect to phase interpolators.

U.S. Pat. No. 5945862 to Donnelly et al.

U.S. Pat. No. 5703905 to Langberg.

U.S. Pat. No. 5554945 to Lee et al.

U.S. Pat. No. 5614855 to Lee et al

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
June 30, 2004

jmp

CHIEH M. FAN
PRIMARY EXAMINER